

Research and Development of a Flash Translation Layer with Demand-based Block-level Address Mapping for Large-Scale NAND Flash Memory Storage Systems (PI: Dr. Shao Zili; 2010/11)

NAND flash memory is widely adopted in the consumer electronics and storage industry. The increasing capacity of NAND flash memory leads to large RAM (main memory) footprint on address mapping in the Flash Translation Layer (FTL) that is a flash management software module embedded inside a flash memory system. This project aims to design and implement a novel FTL with demand-based block-level address mapping for large-scale NAND flash. The objective is to reduce the RAM footprint without sacrificing too much system response time. By doing this, we can reduce the cost of a product with NAND flash memory. Our basic idea is to store the block-level address mapping table in the flash memory and cache on-demand block-level address mapping information into RAM. We will first design a caching system architecture by which we can store the mapping table in the flash and reduce the system response time with caches in RAM. Novel caching schemes will be designed to explore temporal locality, spatial locality and access frequency of workloads. The corresponding address translator, garbage collector and wear leveler of the FTL will be developed. The proposed technique will be implemented based on an embedded software development board with NAND flash memory.